REMARKS/ARGUMENTS

Claims 21 and 22 have been canceled in response to the Examiner's restriction requirement, leaving Claims 1-20, 23 and 24 pending.

The Applicant thanks the Examiner for the telephone interview which she granted on June 23, 2004. In that interview the undersigned pointed out the following, and the Examiner stated that she would consider these arguments.

Claims 1-11, 15-17, 19, 20, 23 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kwan et al. in view of Rice et al. The Applicant respectfully submits that the Examiner has misinterpreted the teachings of Rice et al. and on this basis asks that the Examiner reconsider this rejection.

Claim 1 recites, among other things, "reducing the power supplied to the plasma to a second level lower than the first level to create an idle condition plasma, thereby terminating the processing of the wafer" (emphasis added).

The Examiner states that "Kwan et al. teaches reducing the power supplied to a second level lower than the first level" (Office Action, page 3, lines 16-17). While the Examiner did not cite a specific clause of Kwan et al., the Applicant assumes that she was referring to Table 1 and the accompanying text in column 14 of Kwan et al., which indicates that a total of 6600 W is delivered to the top and side coils (29, 30) during the deposition step and that only 3000 W of power is used to dissociate the etchant gas (col. 14, lines 30-31). Since Kwan et al. supply 3000 W to dissociate the etchant gas, it is evident that they are not supplying the power "to create an idle condition plasma" and that the processing of the wafer has not been terminated.

The Examiner acknowledges that "Kwan et al. does not specifically show creating an idle condition plasma and cooling the wafer in the presence of the idle condition plasma" (Office Action, page 3, lines 15-16). She cites Rice, however, as overcoming this deficiency.

The Examiner states that "Rice et al. discloses the step of creating an idle condition plasma and cooling the wafer in the presence of the idle condition plasma as conventional in the art (Fig. 4B, col. 23, lines 60-67, col. 24, lines 5-45)" (Office Action, page 3, lines 18-20). While Rice et al. does refer to an "idle" mode or condition, it is clear that the plasma is turned off during this period. Thus, Rice et al. states "the plasma chamber has to be

SILICON VALLEY
PATENT GROUP LLP
50 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

switched into an idle mode wherein the plasma is to be kept turned off for an undefined amount of time" (col. 23, line 66, to col. 24, line 1)(emphasis added). Again, referring to Fig. 4B, Rice et al. states "there is no plasma energy being supplied to the kit parts during the idle time period T_2" (col. 24, lines 13-14) (emphasis added). This is directly contrary to Claim 1, which recites "reducing the power supplied to the plasma to a second level lower than the first level to create an idle condition plasma." The complete absence of a plasma (i.e., no plasma at all) cannot reasonably be considered an "idle condition plasma." (See Application, page 4, lines 8) The teaching of Rice et al. is also directly contrary to a key objective of the Applicant's invention, which is "continuously maintaining a plasma condition in the reaction chamber, resulting in the semiconductor wafer being exposed to plasma during transfer" (page 2, lines 27-29). Instead, Rice teaches extinguishing the plasma.

Accordingly, the combination of Kwan et al. and Rice et al. cannot reasonably be interpreted to teach the limitations of Claim 1. Claims 2-20, 23 and 24 depend from Claim 1 and are therefore allowable for the same reasons among others over Kwan et al. in view of Rice et al.

Should the Examiner wish to discuss this case, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 1.

CERTIFICATE OF MAILING BY "FIRST CLASS"

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the below date.

D E Steuber — 6/23/04

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

David E Steuber

David E. Steuber
Attorney for Applicant(s)
Reg. No. 25,557

SILICON VALLEY
PATENT GROUP LLP

50 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210